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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/809,181	03/16/2001	Toshiya Satoh	503.39864X00	5733

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EXAMINER	
DIAZ, JOSE R	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/809,181	SATOH ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 28-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7,8,10,28-33,35 and 36* is/are rejected.

7)☒ Claim(s) *2,6,9 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-4, 28-29, 33 and 35-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagai et al. (US 2002/0130412 A1).

3. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1 and 33, Nagai et al. teaches a semiconductor device comprising: semiconductor elements (1) (see fig. 4) obtained by cutting a semiconductor wafer having an integrated circuit (see paragraph [0029]) and an electrode pad (2) (see fig. 4) formed on one side along a cutting scribe line (consider the boundaries, i.e. each end side, of the substrate 1, as shown in fig. 4), a stress cushioning layer (3) installed on said semiconductor elements (1) (see fig. 4), a lead

wire portion (4) extending from said electrode pad (2) to a top of said stress cushioning layer (3) through an opening (consider the portions of the substrate 1 not covered by the stress cushioning layer 3) formed in said stress cushioning layer on said electrode pad (see fig. 4), external electrode (6) arranged on said lead wire portion on top of said stress cushioning layer (see fig. 4), and a conductor protective layer (5) installed on said stress cushioning layer excluding said external electrode arrange on said lead wire portion (see figs. 2f and 4), wherein said stress cushioning layer (3), said lead wire portion (4), said conductor protective layer (5), and said external electrodes (6) have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line (please note that the stress cushioning layer 3, the lead wire portion 4, the conductor protective layer 5, and the external electrodes 6 do not extend beyond the side boundaries of the semiconductor elements 1, see fig. 2) and exposing a range (the area between the pad 2 and the end side of the substrate 1) from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line, such that said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes are located inside of a peripheral edge of said semiconductor elements (see fig. 2).

Regarding claim 3 and 35, Nagai et al. teaches that the conductor protective layer (5) is formed outside the end face of the stress-cushioning layer (3) (see fig. 4).

Regarding claims 4 and 36, Nagai et al. teaches that the end area (area adjacent to the pad 2) of said stress cushioning layer (3) is formed so as to become tapered and thinner toward the end face of the stress-cushioning layer (3) (see fig. 2).

Regarding claims 28-29, Nagai et al. teaches that the stress-cushioning layer is comprised of a pasty polyimide material or a low elastomeric material (see paragraph [0038]).

4. Claims 1, 3, 28-29, 33 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto (US 2002/0068424 A1).

Regarding claims 1 and 33, Hashimoto teaches a semiconductor device comprising: semiconductor elements (12) (see fig. 1A) obtained by cutting a semiconductor wafer having an integrated circuit (10) and an electrode pad (13) (see fig. 1A) formed on one side along a cutting scribe line (consider the end side S_{12} shown in the Figure 1A, attached below), a stress cushioning layer (22) installed on said semiconductor elements (12) (see fig. 1A), a lead wire portion (18) extending from said electrode pad (13) to a top (T_2) of said stress cushioning layer (22) through an opening formed in said stress cushioning layer on said electrode pad (consider the portion not covered by the stress cushioning layer 22 that include the lead wire portion 18 and electrode pad 13. See fig. 1A, attached below), external electrode (16) arranged on said lead wire portion (18) on top of said stress cushioning layer (T_2) (see fig. 1A), and a conductor protective layer (14) installed on said stress cushioning layer (22) excluding said external electrode arrange (16) on said lead wire portion (18) (see fig. 1A), wherein said stress cushioning layer (22), said lead wire portion (18), said conductor protective layer (14), and said external electrodes (16) have means for forming each end face (End Face) on an end surface of said semiconductor elements inside said cutting scribe

line (S_{12}) and exposing a range (Range) from said end face on said end surface of said semiconductor elements (12) to an inside of said cutting scribe line (S_{12}), such that said stress cushioning layer (22), said lead wire portion (18), said conductor protective layer (14), and said external electrodes (16) are located inside of a peripheral edge (S_{12}) of said semiconductor elements (12) (see fig. 1A, attached below).

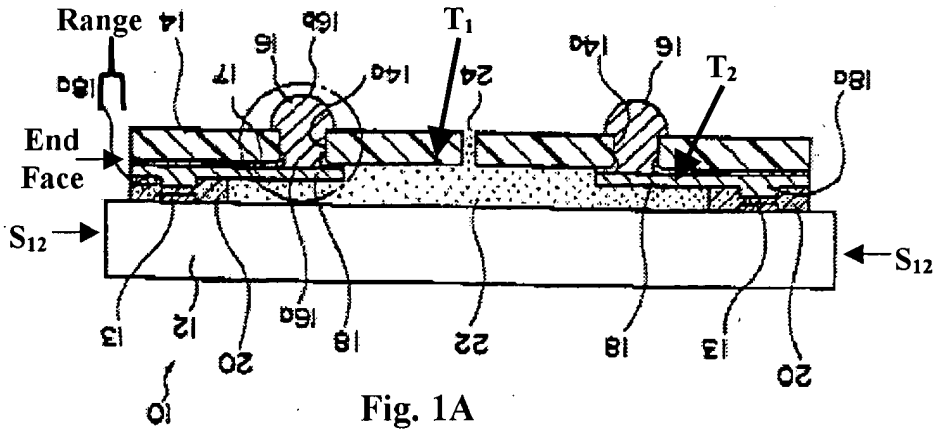


Fig. 1A

Regarding claim 3 and 35, Hashimoto teaches that the conductor protective layer (14) is formed outside the end face of the stress-cushioning layer (22) (see fig. 1A, attached above).

Regarding claims 28-29, Hashimoto teaches that the stress-cushioning layer (22) is comprised of a pasty polyimide material or a low elastomeric material (see paragraph [0109]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 4-5, 7-8, 10, 30-31 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US 2002/0068424 A1) in view of Shimoishizaka et al. (US Pat. No. 6,313,532 B1).

Regarding claim 5, Hashimoto, as stated in the rejection of claims 1 and 33 above, teaches the claimed invention except for the semiconductor element protective layer. Shimoishizaka et al. teaches that it is well known in the art to include a semiconductor element protective layer (12) between the semiconductor elements (10) and the stress cushioning layer (20) (see fig. 7); and a first opening (consider the portion of the substrate 10 not covered by the protective layer 12) in said semiconductor element protective layer (12) on said electrode pad (11) (see figs. 8(a)-8(d)).

With regards to the limitation that the semiconductor element protective layer has an end face on an end surface of said semiconductor elements inside said cutting

scribe line, Hashimoto makes obvious this limitation by showing a patterned structure (consider the structure comprising layers 13, 14, 16, 17, 18 and 22) on the substrate (12), wherein the length of such patterned structure is limited by the length of the exposed surface (Range) of the substrate (12) (see figure 1A, attached above).

Hashimoto and Shimoishizaka et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a semiconductor element protective layer between the semiconductor elements and the stress cushioning layer; and a first opening in said semiconductor element protective layer on said electrode pad, wherein said semiconductor element protective layer has an end face on an end surface of said semiconductor elements inside said cutting scribe line. The motivation for doing so, as is taught by Shimoishizaka et al., is to protecting the semiconductor elements formed on the substrate (col. 3, lines 59-63). Therefore, it would have been obvious to combine Shimoishizaka et al. with Hashimoto to obtain the invention of claims 4-5, 7-8, 10, 30-31 and 36.

Regarding claims 4, 10 and 36, Shimoishizaka et al. teaches that the end area of said stress cushioning layer (20) is formed so as to become tapered and thinner toward the end face of the stress-cushioning layer (20) (see figs. 7 and 8(a)-8(d)). The motivation for doing so is prevention disconnection of the metal wiring layer (col. 3, lines 32-37).

Regarding claim 7, Hashimoto teaches that the conductor protective layer (14) is formed outside the end face of the stress-cushioning layer (22) (see fig. 1A, attached above).

Regarding claim 8, Shimoishizaka et al. teaches that the end face of the semiconductor element protective layer (12) is formed outside the end face of the stress-cushioning layer (20) (see figs. 7 and 8(a)-8(d)).

Regarding claims 30-31, Hashimoto teaches that the stress-cushioning layer (22) is comprised of a pasty polyimide material or a low elastomeric material (see paragraph [0109]).

8. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US 2002/0068424 A1) in view of Shimoishizaka et al. (US Pat. No. 6,313,532 B1), and further in view of Yamamoto (JP 10-092685).

Regarding claim 32, a further difference between the prior art and the claimed invention is the material of the semiconductor element protective layer. Yamamoto teaches that it is well known in the art to form the semiconductor element protective layer (17) of, for example, polyimide (see last two sentences of paragraph [0013] of translation).

Yamamoto, Hashimoto and Shimoishizaka et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further include a semiconductor element protective layer made of, for example, polyimide. The motivation

for further doing so, as is taught by Yamamoto, is reducing the stress (abstract). Therefore, it would have been obvious to further combine Yamamoto with Shimoishizaka et al. and Hashimoto to obtain the invention of claim 32.

Allowable Subject Matter

9. Claims 2, 6, 9 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a device comprising the end face of said conductor protective layer formed inside the end face of said stress cushioning layer; and/or said end face of said semiconductor element protective layer formed inside the end face of said stress cushioning layer.

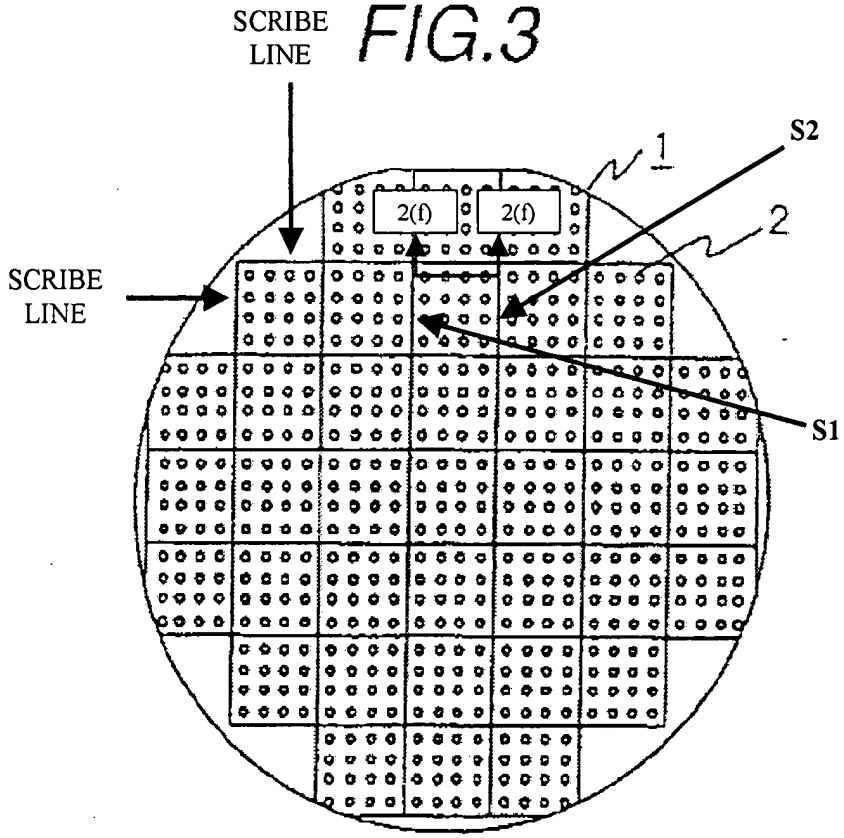
Response to Arguments

11. Applicant's arguments against Shimoishizaka et al., Huang, Yamamoto and Okada et al. references have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Hashimoto. See claim rejections under 35 U.S.C. 102(e) and 35 U.S.C. 103(a) above.

12. Applicant's arguments against the Nagai et al. (US 2002/0130412 A1) reference have been fully considered but they are not persuasive.

Applicant argues that Nagai et al. does not teach end faces of "the stress cushioning layer and the conductor protective layer...positioned inside the cutting scribe line and to be exposed within a range from the end face of the semiconductor element(s) to an inside of the cutting scribe line" (pages 12-13 of remarks). However, the examiner disagrees. It is noted that Applicant used Figure 11 to support his arguments, however the rejection is not based in such figure but by the contrary is based on the teachings shown in Figures 2 and 3. Figure 3 of Nagai et al. shows scribe lines defining the boundaries of each semiconductor device (consider the squares shown in figure 3, attached below), and Figure 2(f) shows a cross sectional view taken, for example, along line 2(f)-2(f) in figure 3 (see figure 3, attached below). Thus, it is clear that the end face (END FACE) of the stress cushioning layer (3), lead wire portion (4), conductor protective layer (5) and external electrode (6) is positioned inside the cutting scribe line (S1) and over the end surface (TOP) of the semiconductor elements (1) so that a range (RANGE) is exposed from said end face (END FACE) to an inside of said cutting line (S1) (see Figure 2(f), attached below). Therefore, the rejection of claims 1, 3-4, 28-29, 33 and 35-36 in view of Nagai et al. is considered to be proper.

FIG.3


SCRIBE LINE
SCRIBE LINE
1
S2
2
2(f)
2(f)
S1

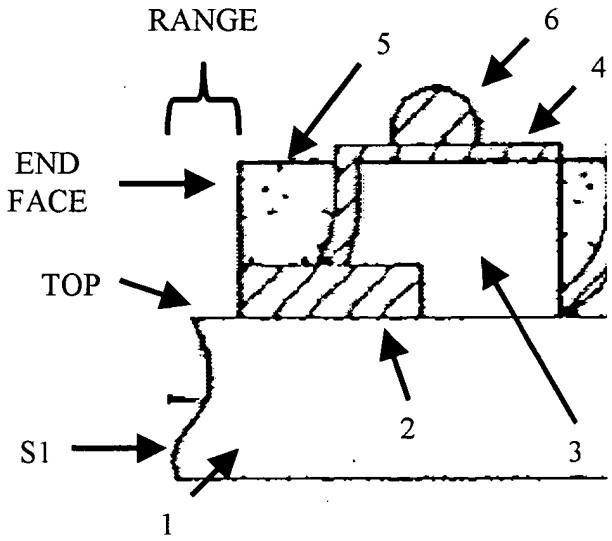

RANGE
5
6
4
END FACE
TOP
2
3
S1
1

FIG. 2(f)

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
11/13/04

Tom Thomas

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